Computer Engineering Technology
2014-15 Assessment Report

I. Introduction

In 1965, OIT was invited to join a Technical Education consortium sponsored by a number of major computer manufacturers. In response, OIT developed an Electro-Mechanical Engineering Technology program. This program was based on a mix of existing EET, MET, Math and other support courses. The name of the program was changed to Computer Systems Engineering Technology in 1973 in order to better represent the course material and capabilities of graduates. Course offerings were expanded, refined and renumbered using CST prefixes to reflect their computer systems content. Since that time, the program has continued to evolve in order to track new developments in the field and keep graduates current. As of this time, the program is only offered on the Klamath Falls campus. Enrollment in the department continued to be flat or up slightly relative to previous years, but, the number of students selecting to pursue a degree in CET was up a little from the previous year. Three students graduated with BS degrees and 6 students were awarded AE degrees in the June 2015 commencement. The results of the 2014 graduate success survey showed a starting salary range of $63,500-66,500. During the academic year, we hired a new faculty member, Kevin Pintong, to replace a retiring faculty member, Ralph Carestia.

II. Summary of program mission, educational objectives and student learning outcomes

The program educational objectives and student learning outcomes are reviewed annually (each fall) by the program faculty and by our IAB. This year, during an ABET accreditation visit, the visitors formally expressed a concern that certain terms used in ABET general criteria a – k were not apparent in our program ISLOs. For example we were cited for not adding the term "analyze" to ISLO 2 and for not adding the phrase "and a respect for diversity" to ISLO 4 (among other similar deficiencies). To address these concerns, we decided to simply adopt the ABET general program a – k outcomes (and by extension, the program specific outcomes for CET) as our ISLOs for all programs in CSET. This also has an additional advantage of harmonizing the ISLOs of all programs in CSET. This change, along with the current mission and PEOs were presented to the IAB and approved at a Dec 5 meeting. Our assessment activities for 2014-15 were subsequently adjusted to reflect this change.

Mission

The mission of the Computer Engineering Technology (CET) Degree program in the Computer Systems Engineering Technology (CSET) Department at Oregon Institute of Technology is to provide an excellent education incorporating industry-relevant, applied laboratory based design and analysis to our students. The program is to serve a constituency consisting of its Alumni, employers in the high-technology industry, and the members of our IAB. Major components of the CET program's mission in the CSET Department are to:

I. educate computer engineering technology students to meet current and future industrial challenges,

II. promote a sense of scholarship, leadership, and professional service among our graduates,

III. enable our students to create, develop, and disseminate knowledge for the applied engineering environment,

IV. expose our students to cross-disciplinary educational programs, and provide high tech industry employers with graduates in the computer engineering technology profession, a profession which is increasingly being driven by advances in technology.

CET Program Educational Objectives

Program Educational Objectives are broad statements that describe what graduates are expected to attain within a few years of graduation.

Alumni of the Computer Engineering Technology (CET) Bachelor Degree program may be employed in a wide range of high tech industries from industrial manufacturing to consumer electronics where they will be involved in solving problems through the development of hardware, software and embedded applications. Alumni may be involved in product design, testing and qualification, application engineering, customer support, sales, or public relations.

A) Alumni will demonstrate technical competency through success in computer engineering technology positions and/or pursuit of engineering or engineering technology graduate studies if desired.

B) Alumni will demonstrate competencies in communication and teamwork skills by assuming increasing levels of responsibility and/or leadership or managerial roles.

C) Alumni will develop professionally, pursue continued learning and practice responsibly and ethically.

Alumni of the Computer Engineering Technology (CET) Associate Degree program may be employed as technicians or in support roles in a wide range of high tech industries from industrial manufacturing to consumer electronics. Alumni may be involved in product testing and qualification, customer support, sales, or public relations.

A) Alumni will demonstrate technical competence through success in computer engineering technician positions.

B) Alumni will demonstrate competencies in communication and teamwork skills through positive contributions to team based engineering projects.

C) Alumni will develop professionally, pursue continued learning and practice responsibly and ethically.

According to current statistics, one third of students who obtain the CET Associate degree also obtain a Bachelor degree in a related discipline, most often a Bachelor degree in Software. In this case, the Associate degree adds breadth to their education. Alumni in this category would be expected to perform at a level consistent with the Bachelor degree program educational objectives.

CET Bachelor of Science Program Student Learning Outcomes

Graduates of the CET Bachelor's degree program are expected to be able to demonstrate:

1. an ability to select and apply the knowledge, techniques, skills, and modern tools of the discipline to broadly-defined engineering technology activities;

2. an ability to select and apply a knowledge of mathematics, science, engineering, and technology to engineering technology problems that require the application of principles and applied procedures or methodologies;

3. an ability to conduct standard tests and measurements; to conduct, analyze, and interpret experiments; and to apply experimental results to improve processes;

4. an ability to design systems, components, or processes for broadly-defined engineering technology problems appropriate to program educational objectives;

5. an ability to function effectively as a member or leader on a technical team;

6. an ability to identify, analyze, and solve broadly-defined engineering technology problems;

7. an ability to apply written, oral, and graphical communication in both technical and non-technical environments; and an ability to identify and use appropriate technical literature;

8. an understanding of the need for and an ability to engage in self-directed continuing professional development;

9. an understanding of and a commitment to address professional and ethical responsibilities including a respect for diversity;

10. a knowledge of the impact of engineering technology solutions in a societal and global context; and

11. a commitment to quality, timeliness, and continuous improvement.

CET Associate Degree Student Learning Outcomes

Graduates of the CET Associate degree program are expected to be able to demonstrate:

1. an ability to apply the knowledge, techniques, skills, and modern tools of the discipline to narrowly defined engineering technology activities;

2. an ability to apply a knowledge of mathematics, science, engineering, and technology to engineering technology problems that require limited application of principles but extensive practical knowledge;

3. an ability to conduct standard tests and measurements, and to conduct, analyze, and interpret experiments;

4. an ability to function effectively as a member of a technical team;

5. an ability to identify, analyze, and solve narrowly defined engineering technology problems;

6. an ability to apply written, oral, and graphical communication in both technical and non-technical environments; and an ability to identify and use appropriate technical literature;

7. an understanding of the need for and an ability to engage in self-directed continuing professional development;

8. an understanding of and a commitment to address professional and ethical responsibilities, including a respect for diversity; and

9. a commitment to quality, timeliness, and continuous improvement.

III. Assessment Cycle

The assessment cycle appears below. For the BS program, four of the 12 student learning outcomes are assessed each year of a three year cycle. For the AE program, the outcomes that correspond to the BS program outcomes are assessed.

CET BS Program Assessment Plan

Learning Outcome:	14-15	15-16	16-17
1. an ability to select and apply the knowledge, techniques, skills, and modern tools of the discipline to broadly-defined engineering technology activities		•	
2. an ability to select and apply a knowledge of mathematics, science, engineering, and technology to engineering technology problems that require the application of principles and applied procedures or methodologies	•		
3. an ability to conduct standard tests and measurements; to conduct, analyze, and interpret experiments; and to apply experimental results to improve processes	•		
4. an ability to design systems, components, or processes for broadly-defined engineering technology problems appropriate to program educational objectives;		•	
5. an ability to function effectively as a member or leader on a technical team		•	
6. an ability to identify, analyze, and solve broadly-defined engineering technology problems	•		
7. an ability to apply written, oral, and graphical communication in both technical and non-technical environments; and an ability to identify and use appropriate technical literature			•
8. an understanding of the need for and an ability to engage in self-directed continuing professional development			•
9. an understanding of and a commitment to address professional and ethical responsibilities including a respect for diversity		•	
10. a knowledge of the impact of engineering technology solutions in a societal and global context			•
11. a commitment to quality, timeliness, and continuous improvement		•	

CET AE Program Assessment Plan

Learning Outcome:	14-15	15-16	16-17
1. an ability to apply the knowledge, techniques, skills, and modern tools of the discipline to narrowly defined engineering technology activities		•	
2. an ability to apply a knowledge of mathematics, science, engineering, and technology to engineering technology problems that require limited application of principles but extensive practical knowledge	•		
3. an ability to conduct standard tests and measurements, and to conduct, analyze, and interpret experiments;	•		
4. an ability to function effectively as a member of a technical team;		•	
5. an ability to identify, analyze, and solve narrowly defined engineering technology problems;	•		
6. an ability to apply written, oral, and graphical communication in both technical and non-technical environments; and an ability to identify and use appropriate technical literature;			•
7. an understanding of the need for and an ability to engage in self-directed continuing professional development			•
8. an understanding of and a commitment to address professional and ethical responsibilities including a respect for diversity		•	
9. a commitment to quality, timeliness, and continuous improvement		•	

IV. Summary of 2014-15 Assessment Results

During the 2014-15 academic year, the program faculty assessed three student learning outcomes as summarized below. These outcomes are mapped to the CET curriculum in Appendix A.

Student Learning Outcome #2 (BS degree): an ability to select and apply a knowledge of mathematics, science, engineering, and technology to engineering technology problems that require the application of principles and applied procedures or methodologies.

Student Learning Outcome #2 (AE degree): an ability to apply a knowledge of mathematics, science, engineering, and technology to engineering technology problems that require limited application of principles but extensive practical knowledge.

Direct Assessment #1

This assessment focuses on the application of K-Map techniques to a logic minimization problem.

Data Collection Date: 11/05/14

Coordinator: Phong Nguyen

Assessment Method: Students (32 total) in CST 162 were given a set of specifications to a digital logic design problem. They are next required to follow a specific method to come up with a design which they are to implement using gates. At the end, the students are asked to check a truth table to partially check functionality of the design. Student work was assessed in each of the following performance criteria as defined in the attached rubric.

Performance Criteria	Measurement Scale	Minimum Acceptable Performance	Results
Understanding Specifications	1-4 according to rubric	70% at 3 or 4	31/32 = 96.9%
Plan to Solve	"	"	32/32 = 100%
Carry out Plan	"	"	26/32 = 81.3%
Evaluating	"	"	27/32 = 84.4%
Solution	"	"	30/32 = 93.4%

Evaluation (6/3/2015): The performance passed standard. This represents an improvement over the last time this assessment was given. The increased focus on recognizing redundant loops in K-maps appears to have paid off.

Actions (6/3/2015): No changes need to be made as a result of this assessment.

Direct Assessment 2

This assessment focused on problem formulation.

Data Collection Date: 02/06/15

Coordinator: Douglas W. Lynn

Assessment Method: A question (6d) was given on the CST 442 midterm exam that required students to compute the change in CPI from making jumps take one cycle as opposed to two. To correctly solve this problem, students have to realize that CPIold = $1.17 = x + .02 \times 2$, and that what they want is CPInew = $x + .02 \times 1 = 1.17 - .02 \times 1 = 1.15$.

Performance Criteria	Measurement Scale	Minimum Acceptable Performance	Results
Correct Formulation	number of errors	70% correct formulation	100% (3/3) had a correct formulation

Evaluation (6/3/2015): Performance exceeded expectations, doing much better than the last time this assessment was given.

Actions (6/3/2015): No changes need to be made as a result of this assessment.

Direct Assessment #3

This assessment focused on the application of basic probability.

Data Collection Date: 3/12/15

Coordinator: Douglas W. Lynn

Assessment Method: The following question was given in the CST 418 (Networks) final exam:

If the probability of an error in one packet of a message traversing one hop of a network is Pe, what is the probability that N packets can be delivered across an n hop virtual circuit without any errors? To correctly solve this problem students must realize that Pne = 1 - Pe, that N x n packets have without to be transmitted error and that probabilities multiply.

Performance Criteria	Measurement Scale	Minimum Acceptable Performance	Results
Pne = 1 - Pe	correct / incorrect (or not attempted)	70% correct	100% (3/3)
Probabilities multiply	correct / incorrect (or not attempted)	70% correct	100% (3/3)

Evaluation (6/3/2015): Performance exceeded expectations.

Actions (6/3/2015): No changes need to be made as a result of this assessment.

Indirect Assessment #1

Data Collection Date: Spring 2015

Coordinator: Doug Lynn

7 of 8 CET seniors responding on the 2012-13, 2013-14 and 2014-15 senior exit survey questions related to this outcome judged that they were adequately prepared with an ability to select and apply a knowledge of mathematics, science, engineering, and technology to engineering technology problems that require the application of principles and applied procedures or methodologies. identifying and solving computer engineering technology problems.

Actions (6/30/2015): No changes need to be made as a result of this assessment

Student Learning Outcome #3 (BS degree): an ability to conduct standard tests and measurements; to conduct, analyze, and interpret experiments; and to apply experimental results to improve processes.

Student Learning Outcome #3 (AE degree): an ability to conduct standard tests and measurements, and to conduct, analyze, and interpret experiments.

Direct Assessment #1

Data Collection Date: 3/05/15

Coordinator: Phong Nguyen

Assessment Method: Students (11 total) in CST 162 were given a lab in which series and parallel circuits were built and measurements were taken for voltage, current and resistance. The measurements are compared against theoretical values which the students must calculate. Student work was assessed in each of the following performance criteria as defined in the attached rubric.

Performance Criteria	Measurement Scale	Minimum Acceptable Performance	Results
Calculate theoretical values for series and parallel circuits	1-4 according to rubric	70% at 3 or 4	11/11 = 100%
Build a series circuit on Digital trainer	"	"	11/11 = 100%
Build a parallel circuit on Digital trainer	"	"	11/11 = 100%
Measure voltage using multimeter	"	"	11/11 = 100%
Measure current using multimeter	"	"	11/11 = 100%
Measure resistance using multimeter	"	"	11/11 = 100%
Analyze measured compared to theoretical values	"	"	11/11 = 100%

Evaluation (6/3/2015): Performance exceeded the standard in all performance criteria.

Actions (6/3/2015): No changes need to be made as a result of this assessment.

Direct Assessment #2

This assessment focused on the ability to conduct standard measurements.

Data Collection Date: 3/12/15

Coordinator: Douglas W. Lynn

Assessment Method: Students in CST 331 were required to use a logic analyzer to identify and measure (among other parameters) setup (Tdw) and hold (Tdh) provided to a static RAM chip by a PIC32 processor and the setup (PM6) and hold (PM7) provided to a PIC32 processor by the RAM chip. They were required to actually measure all setups, but to either measure the holds or justify that the hold requirements were met.

Performance Criteria	Measurement Scale	Minimum Acceptable Performance	Results
Student was able to properly setup the logic analyzer	Able / needed assistance	100% able	100% (5/5)
Tdw correctly identified and measured.	correct / incorrect (or not attempted)	70% correct	100% (5/5)
PM6 correctly identified and measured.	correct / incorrect (or not attempted)	70% correct	80% (4/5)
Tdh correctly identified and measured or justified.	correct / incorrect (or not attempted)	70% correct	80% (4/5)
PM7 correctly identified and measured or justified.	correct / incorrect (or not attempted)	70% correct	60% (3/5)

Evaluation (6/3/2015): Performance exceeded expectations with the exception of PM7. Several students assumed since the PM7 requirement was 0 ns min, they did not have to make the measurement or to clearly justify that the requirement was met.

Actions (6/3/2015): Next time the assessment is given, more emphasis will be placed on having a clear justification for hold times that is backed up with a screen capture. Otherwise, no changes need to be made as a result of this assessment.

Indirect Assessment #1
Data Collection Date: Spring 2015
Coordinator: Doug Lynn

8 of 8 CET seniors responding on the 2012-13, 2013-14 and 2014-15 senior exit survey questions related to this outcome judged that they were adequately prepared with an ability to conduct standard tests and measurements; to conduct, analyze, and interpret experiments; and to apply experimental results to improve processes.

Actions (6/30/2015): No changes need to be made as a result of this assessment.

Student Learning Outcome #6 (BS degree): an ability to identify, analyze, and solve broadly-defined engineering technology problems

Student Learning Outcome #5 (AE degree): an ability to identify, analyze, and solve narrowly defined engineering technology problems.

Direct Assessment #1

Data collection Date: 2/15/2015

Coordinator: Kevin P. Pintong

Assessment Method: Students in CST451 were required to debug a circuit board made with schematic errors. Errors on this circuit board based on the Spartan 6 FPGA and M25P80 EEPROM. The Spartan 6 FPGA BOM incorrectly referenced U2 and U3, and the M25P80 had multiple incorrectly wired pins. Students were provided materials to build the board, the schematic, layout, and a bill of materials. Students were encouraged to use part datasheets.

Performance Criteria	Measurement Scale	Minimum Acceptable Performance	Results
Student correctly identified components U1 and U3 were swapped in the BOM.	Correct, Incorrect, Not Attempted	70% correct	100% (2/2)
Student identified EEPROM was wired incorrectly	Correct, Incorrect, Not Attempted	70% correct	100% (2/2)
Student was able to extrapolate data from datasheet to determine the correct wiring configuration for EEPROM.	1 = Student cannot identify or correct errors in the EEPROM wiring. 2 = Does not identify all incorrectly routed pins and/or misidentifies some correctly routed pins as being incorrectly routed. 3 = Identifies incorrectly routed pins. Does not provide an acceptable solution. 4 = Identifies incorrectly routed	70% of students performing at 3 or 4	100% (2/2)

	pins. Provides acceptable solution for EEPROM layout.		
Student does not (incorrectly) identify correct design features as an error.	1 = More than four features identified as errors. 2 = Four features identified as errors. 3 = Two to three features identified as errors. 4 = No features identified as errors.	70% of students performing at 3 or 4	100% (2/2)

Evaluation 6/10/2015: Performance exceeded expectations, however there is a small sample size.
Actions 6/10/2015: No actions are required as a result of this assessment.

Indirect Assessment #1
Data Collection Date: Spring 2015
Coordinator: Doug Lynn

8 of 8 CET seniors responding on the 2012-13, 2013-14 and 2014-15 senior exit survey questions related to this outcome judged that they were adequately prepared with an ability to identify, analyze, and solve broadly-defined engineering technology problems.

Actions (6/30/2015): No changes need to be made as a result of this assessment.

V. Summary of Student Learning

This year, student performance in all assessed objectives exceeded expectations in all performance criteria except one. In this one case, direct assessment #2 for outcome #3, students did not demonstrate their ability to measure a specified hold time using a logic analyzer. Next time the assessment is given, more emphasis will be placed on having a clear justification for hold times that is backed up with a screen capture.

VI. Changes Resulting from Assessment

In this assessment cycle, students demonstrated an improved ability in outcome #2 (applying knowledge to the solution of problems) compared to the previous time this outcome was

assessed. The increased focus on recognizing redundant loops in K-maps, recommended as a result of the previous assessment, appears to have paid off.

Appendix A: SLO Curriculum Maps

Outcome Assessment Points, BS Program H = Highly assessable M = Weakly assessable blank = Low to not assessable		(1) problem solving	(2) experiment	(3) teamwork	(4) ethical / social resp	(5) life-long learning	(6) calc, prob, discrete	(7) master skills + knowledge	(8) design, analysis, sim	(9) design, fab, test, improve	(10) oral presentation	(11) written presentation	(12) quality, proj. manage
Freshman Year	Eval. Cycle ⇨	Y1	Y2	Y3	Y3	Y2	Y1	Y3	Y2	Y1	Y3	Y2	Y3
CST 102	Intro to Comp Sys	M	M	M	M					M		M	
CST 162	Intro to Digital Logic	H	M				M						
Math 111	College Algebra												
WRI 121	English Comp												
PSY 201	Psychology												
CST 116	C++ Prog I												
CST 130	Computer Org						M						
Math 112	Trigonometry												
WRI 122	Argumentative Writing												
HUM	Hum Elective												
CST 105	Intro to Comp Sys III				M								
CST 126	C++ Prog II												
CST 131	Comp Arch						M						
MATH 251	Diff Calculus						M						
SPE 111	Public Speaking										M		
Sophomore Year													
CST 250	Assembly Lang												
MATH 252	Integral Calculus						M						
WRI 227	Tech Report											M	
CST 133	Dig Elec II – Seq w HDL						M			M			
CST 134	Instrumentation		M						M				
CST 204	Intro to µcontrollers						M		M	M			
EE 221	DC & 1st Ord Trans		M				M	M					
CST 231/2	Comp Des w/PLD	M	H			M	M		M	H			
Math 254N	Vector Calc						H						
CST 240	Unix	M	M				M	M	M	M			
EET 237/8	AC & 2nd Ord Trans		M				M	M					
SPE 321	Team Comm			M							H		
Math	Math Elective						H						

Outcome Assessment Points, BS Program continued		(1) problem solving	(2) experiment	(3) teamwork	(4) ethical / social resp	(5) life-long learning	(6) calc, prob, discrete	(7) master skills + knowledge	(8) design, analysis, sim	(9) design, fab, test, improve	(10) oral presentation	(11) written presentation	(12) quality, proj. manage
Junior Year	Eval. Cycle ⇨	Y1	Y2	Y3	Y3	Y2	Y1	Y3	Y2	Y1	Y3	Y2	Y3
CST 337	Embedded Sys Arch	M	M				M	M	M	M		H	
CST 335	I/O Interfacing	M	M	M		M				M			
CST 371	Embedded Sys Dev I	H	M	H		M			H	M	H	H	M
PHY 221	Physics w/Calculus												
CST 331	Microproc Interface	M	M				M	M	M	M		M	
CST 372	Embedded Sys Dev II	H	M	H		M	M	M	H	H	M	M	M
PHY 222	Physics w/Calculus												
EET 308/9	MOS Microelectronics		M				M	M					
CST 351	Advanced PLDs	H	H		M	M		M	H	M			M
CST 373	Embedded Sys Dev III	H	H	H	M	H	M	M	M	H	H	H	H
PHY 223	Physics w/Calculus												
HUM	Hum Elective				M								
WRI 327	Adv Tech Writing											H	
Senior Year													
BUS 304	Engr Management				M								
CST 344	Intermediate Arch	M			M		M	M	M	M			
CST 441	Logic Synth w VHDL	H	H		M	M		H	H	M			
CST xxx	Tech Elective					M							
SSC	SS Elective				M								
CST 442	Advanced Arch.	M				M	H	H	M	M			
CST 451	ASIC Des using FPGAs	H	H		M	M		H	M	H	H	H	M
CST 418	Data Comm & Net	M				M	H						
SSC	SS Elective				M								
MGT 345	Engr Economy				M								M
CST 464	RISC-Based µproc	M	M	M		M		M	M	M			
CST 461	Adv Topics in VLSI	M	H				M	H	H			M	
Anth 452	Globalization				M								
HUM	Hum Elective				M								

Outcome Assessment Points, AE Progam H = Highly assessable M = Weakly assessable blank = Low to not assessable		(1) problem solving	(2) experiment	(3) teamwork	(4) ethical / social resp.	(5) life-long learning	(6) calc, discrete	(7), analysis, sim, test	(8) fabricate, test	(9) oral presentation	(10) written presentation
Freshman Year	Eval. Cycle ⇨	Y1	Y2	Y3	Y3	Y2	Y1	Y2	Y1	Y3	Y2
CST 102	Intro to Comp Sys.	M	M	M					M		M
CST 162	Intro to Digital Logic	H	M				M				
MATH 111	College Algebra										
WRI 121	English Composition										
PSY 201	Psychology										
CST 116	C++ Programming I										
CST 130	Computer Organization						M				
MATH 112	Trigonometry										
WRI 122	Argumentative Writing										
HUM	Humanities Elective				M						
CST 105	Intro to Comp Sys. III				M						
CST 126	C++ Programming II										
CST 131	Computer Architecture						M				
MATH 251	Differential Calculus						M				
SPE 111	Fundamentals of Speech									M	M
Sophomore Year											
CST 250	Computer Assembly Language										
MATH 252	Integral Calculus						M				
WRI 227	Technical Report Writing										M
CST 133	Dig. Elec. II – Seq. Logic w HDL						M				
CST 134	Instrumentation		M					M	M		
CST 204	Introduction to µcontrollers						M				
EE 221	Circ. I – DC & 1st Order Trans.										
CST 231	Computer Design w/PLD	M	H			M	M	M	H		
CST 232	Comp. Design w/PLD Lab	H	H			M	M	M	H		
PHY 221	General Physics w/Calculus										
CST 240	Unix	M	M				M	M	M		
EET 237/8	Circ. II – AC & 2nd Order Trans.										
PHY 222	General Physics w/Calculus										
SSC	SS Elective				M						